PATENT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Applicant:	FOO ET AL.	)	Examiner V. Kovalick
Appl. No.	10/647,723	)	Art Unit 2629
Confirm. No.	2166	)	Atty. Docket No. CS22497RA
Filed:	25 August 2003	)	

Title: "Matrix Display Having Addressable Display Elements And Methods"

PRE-APPEAL BRIEF REVIEW REQUEST

Assistant Commissioner for Patents
Alexandria, Virginia 22313

Sir:

Request for Reconsideration, Claims Pending

The final Office action mailed on 20 March 2007 has been considered carefully. A pre-brief conference is requested. A notice of appeal has been filed concurrently. The Claims have not been amended subsequent to the mailing of the final rejection.

Claims 5, 7-9, 17 and 19-20 are allowed. Claims 2-3 and 13-15 were indicated as being allowable but stand objected to for dependence on a rejected base or intermediate claim.

Claims 1-5, 7-17 and 19-20 are pending.

Allowability of Claims Over Yasukawa, Crossland & Hilbrink

Rejection Summary

Claim 1 stands rejected under 35 USC 103(a) as being unpatentable over U.S. Publication No. 2003/0210363 (Yasukawa) in view of U.S. Patent No. 5,408,248 (Crossland) and U.S. Patent No. 4,641,135 (Hilbrink).

Discussion of Claim 1

Regarding Claim 1, the prior art fails to disclose or suggest a

> … method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch, the method comprising:
> applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element;
> applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element;
> activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Contrary to the Examiner's assertion, there is no motivation or suggestion to combine Yasukawa, Crossland and Hilbrink as alleged by the Examiner. The Examiner's assertion (p. 7, para. 9, Office action of 22 March 2007) that the motivation to combine references is "… found in the knowledge generally available …" is not supported by the prior art.

Yasukawa reduces flickering and degradation of image quality caused by stray light in a TFT switched display by forming a light shield over

a channel region of each TFT. Yasukawa also connects a capacitor (70) in parallel with each TFT to reduce leakage of the image signal. Crossland teaches reducing cumulative charge imbalance effects by refreshing an LCD cell by applying a voltage with a reversing polarity. Hilbrink discloses the use of diode pairs to charge and discharge a field effect picture element.

It's questionable whether the LCD voltage polarity reversing scheme of Crossland would be suitable for driving the active matrix display of Yasukawa, thus raising doubt over whether the putative combination would have had a reasonable expectation of success. It's not even clear that the display of Yasukawa suffers from the problem addressed by Crossland. Also, the diode-based pixel driver system of Hilbrink is not suitable for driving the TFT driven cells of Yasukawa or the LCD array of Crossland.

The asserted combination of Yasukawa, Crossland and Hilbrink nevertheless fails to disclose or suggest an n x m array of display elements wherein each display element is coupled "to a logic controlled switch". Moreover, none of the references cited disclose "... activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition" as recited in Claim 1. Claim 1 is thus patentably distinguished over the art.

Allowability of Claims Over Yasukawa, Crossland, Hilbrink & Martin

Rejection Summary

Claims 10-12 and 16 stand rejected under 35 USC 103(a) as being unpatentable over Yasukawa in view of Crossland, Hilbrink and Martin.

Allowability of Claim 10

Regarding Claim 10, the prior art fails to disclose or suggest a

> … display device comprising:
> a plurality of display elements arranged in a matrix,
> each display element including a display pixel coupled to a switch,
> each display element including an addressable latch having an output coupled to a controlling input of the switch,
> the addressable latch having a row address input and a column address input.

Contrary to the Examiner's assertion, there is no motivation or suggestion to combine Yasukawa, Crossland and Hilbrink as alleged by the Examiner. The Examiner's assertion that the motivation to combine references is "… found in the knowledge generally available …" is unsupported.

Yasukawa reduces flickering and degradation of image quality caused by stray light in a TFT switched display by forming a light shield over a channel region of each TFT. Yasukawa also connects a capacitor (70) in parallel with each TFT to reduce leakage of the image signal. Crossland teaches reducing cumulative charge imbalance effects by refreshing an LCD cell by applying a voltage with a reversing polarity. Hilbrink discloses the use of diode pairs to charge and discharge a field effect picture element.

It's questionable whether the LCD voltage polarity reversing scheme of Crossland would be suitable for driving the active matrix display of

Yasukawa, thus raising doubt over whether the putative combination would have had a reasonable expectation of success. It's not even clear that the display of Yasukawa suffers from the problem addressed by Crossland. Also, the diode-based pixel driver system of Hilbrink is not suitable for driving the TFT driven cells of Yasukawa or the LCD array of Crossland.

The asserted combination of Yasukawa, Crossland, Hilbrink and Martin nevertheless fails to disclose or suggest a plurality of display elements arranged in a matrix wherein each display element includes "... an addressable latch having an output coupled to a controlling input of the switch..." and wherein "... the addressable latch having a row address input and a column address input..." as recited in Claim 10. Martin teaches pipelined memory, which is unrelated to the subject matter of Claims 10-12 and 16. Claim 10 is thus patentably distinguished over the art.

Prayer For Relief

In view of the discussion above, all Claims of the present application are in condition for allowance. Kindly withdraw any rejections and allow this application to issue as a United States Patent without delay.

Respectfully submitted,

/ R K Bowler/

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ROLAND K. BOWLER II 27 MAR. 2007
REG. NO. 33,477

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